REMARKS

Although the Action is indicated as being final, it is noted that rejections under 35 U.S.C. 101 and 35 U.S.C. 112 are presented for the first time notwithstanding that no claim amendments were presented. In this connection, during an interview with the Examiner on February 9, 2004, the Examiner acknowledged that the finality of the Action was improper and stated that such finality would be withdrawn. Accordingly, Applicant is proceeding with this response based upon the Action being non-final.

Rejections Under 35 U.S.C. 101

Claims 1-13 are rejected under 35 U.S.C. 101, the Examiner contending that the language of the claims raises a question as to whether the claims are directed to merely an abstract idea that is not tied to a technological art, environment or machine which would result in a practical application producing a concrete, useful and tangible result to form the basis for statutory subject matter under 35 U.S.C. 101. The Examiner contends that the claims merely state items comprised onto a data management system and do not state what is being performed and thus there is lack of utility. In response, Applicant notes that 35 U.S.C. 101 states:

> Whoever invents or discovers any new and useful process, machine, manufacturer or composition of matter, or any new and useful improvement thereof, may obtain a patent therefore, subject to the conditions and requirements of this title.

Since the statute makes no reference to a requirement that the claims may not be "directed to merely an abstract idea that is not tied to a technological art . . ." Applicant submits that the Examiner has misconstrued 35 U.S.C. 101. Further, Applicant submits that the interconnected claim elements XOR engine, host/network interface, cache and storage device are a machine and therefore in compliance with 35 U.S.C. 101. Accordingly, reconsideration and withdrawal of the rejection of the claims under 35 U.S.C. 101 is requested.

Claim Objections

Claims 1-13 are objected to, the Examiner contending that the use of the term "cache" should be replaced with "cache memory." In response, Applicant notes that persons skilled in the art, upon reading this specification, would recognize that the reference to cache is its ordinary dictionary meaning when applied to the computer arts, namely a small, fast memory holding recently accessed data designed to speed up subsequent access to the same data. Thus, there is nothing unclear about the use of the term "cache" in the claims which would be cleared up by use of the term "cache memory." Accordingly, reconsideration and withdrawal of this objection is requested.

Rejections Under 35 U.S.C. 112

Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite, the Examiner contending that " the phrase in step (d)'. . . and for coupling to a plurality of storage devices' is not clear." In response, Applicant notes that claim 1 is an apparatus claim and, therefore, has no step (d). However, as to element (d), it is clear from, for example, Figure 2 and the corresponding description in the specification that the storage device interface is coupled to the cache and is designed to be coupled to a plurality of storage devices, hence the claim language "for coupling to . . ." Since the plurality of storage devices do not form part of the invention, it would be inappropriate to state that the storage device interface is coupled to the plurality of storage devices. Claim 6 is rejected for the same reason and, Applicant submits, claim 6 is not indefinite under 35 U.S.C. 112, second paragraph, for the same reasons explained above with respect to claim 1.

The Examiner further contends that in claim 6, "said XOR engine in 'step (sic) (d)'" does not have sufficient antecedent basis. The Examiner further contends that "it doesn't make sense for the 'wherein said XOR . . . ,' to be part of step (sic) (d)." As noted above, the claims are not presented as method claims, and, therefore, the reference to there being a "step (d)" is incorrect. Further, moving "wherein said XOR . . ." to being under step (sic) (a) would result in improper antecedent basis with respect to the terms "host/network interface" and "cache." Claim 7 is rejected for the same reason and Applicant submits that such rejection should be withdrawn for the reasons explained above.

Claim 7 is further rejected under 35 U.S.C. 112 as being indefinite, the Examiner contending that the terms "bus expander" and "bus funnel" are not clear in the claim language. In response, Applicant notes that such terms are clearly defined in the specification with reference to figure 8 and their corresponding description at page 8. Further, Applicant requests that the Examiner take administrative notice of the fact that the terms have well known meanings in the art.

Claims 8, 12 and 13 are rejected under 35 U.S.C. 112, second paragraph, for essentially the same reasons as claims 1, 6 and 7. Applicant requests withdrawal of the rejection under 35 U.S.C. 112, second paragraph, for the reasons explained above with respect to claims 1, 6 and 7.

Rejections Under 35 U.S.C. 102 and 35 U.S.C. 103

Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by DeKoning et al. Claims 2-13 are rejected under 35 U.S.C. 103 as being unpatentable over DeKoning et al., in view of Neufeld. Reconsideration and withdrawal of these rejections are requested in view of the following.

At pages 2-3 of the Action, the Examiner responds to Applicant's prior arguments explaining what the Examiner contends are the teachings of DeKoning et al., and concludes as follows:

> "In particular, DeKoning et al., teaches (Figures 1 and 2) the XOR engine (62) coupled to the memory controller (60), which is analogous to the host/network interface of the present application. The memory controller (60) is also coupled to the PCI bus (28)."

The host/network interface of the present invention is shown in block diagram form in Figure 5 with corresponding description at pages 4 and 5. For example, at page 4, Applicant defines host/network interface 31 as:

> "a communications interface to a host computer or a network of computers. In one embodiment, the invention maintains a ANSI-X3T11 fiber channel interface utilizing a SCSI command set on the front end . . ."

RPA memory controller 60 of DeKoning et al. is not analogous to Applicant's host/network interface. In particular, DeKoning et al. clearly shows RPA memory controller 60 connected to system PCI bus 28 and not for coupling to a host computer system as claimed by Applicant. Although not shown in Figure 2, it is apparent that PCI bus 28 is the same PCI bus 28 shown in Figure 1. For example, in column 4, line 42, it is stated "The RPA memory controller 60 controls (1) the flow of data between the system bus 28 . . . ." It is apparent that Figure 2 is not a complete system diagram, but rather the elements shown above bus 28 in Figure 1, which include host interface 16 also exist in the system of Figure 2 even though not shown. To the extent that there is an analogous element in DeKoning et al., to Applicant's host/network

interface, it is host interface 16 which is shown as being connected to host device 3. For example, in Column 6 of DeKoning et al., it is stated at line 26:

"chunk 4 is transferred from the host device 31, through a host interface circuit 16, across the system bus 28, through the RPA memory controller 60."

As stated by the Examiner, at page 2 of the Action:

"RPA memory controller 60 controls (1) the flow of data between the system bus 28, the RPA memory 22 and the intermediate memory parity buffer 64 . . . ,"

Such functions have absolutely nothing to do with translating and decoding data and non-data commands transmitted over a fiber channel or TCP/IP or Ethernet interface or the like which is the function provided by Applicant's host/network interface as explained at pages 4-5 of the Application.

In further responding to Applicant's argument, the Examiner states:

"Applicants contend, . . . in Applicant's claim 2, the claimed logic means is for generating an XOR parity byte, checking and correcting detected parity errors . . .

The Examiner respectfully disagrees."

It is unclear what the Examiner disagrees with since Claim 2 clearly states that the logic means is for:

"generating an XOR parity byte using said data and appending said parity byte to said data, checking XOR parity and correcting detected parity errors."

For this reason, the Examiner's contention that Neufeld teaches a dedicated XOR engine which generates parity data on a word for word basis from up to four different transfer blocks and is capable of writing the result to a specified drive or to a transfer offered through a sub-channel is irrelevant since there is no teaching of detecting and correcting parity errors. More

particularly, Applicants prior argument concerning the claimed logic means was responding to the Examiner's prior contention that Neufeld's trap logic 300 corresponds to the claimed logic means. The Examiner's reference to the teachings of Neufeld at column 2 states that there is an XOR engine which generates parity data and writes the result to a specified drive for a transfer buffer. There is no mention of checking or correcting detected parity errors.

Moreover, DeKoning et al. does not contain teachings concerning an XOR engine and a host/network interface coupled to the XOR engine. Since Neufeld also does not contain these teachings, the combination of DeKoning et al. and Neufeld cannot result in the present invention.

In view of the foregoing, reconsideration and withdrawal of the various rejections under 35 U.S.C. 101, 35 U.S.C. 102, 35 U.S.C. 103 and 35 U.S.C. 112 and issuance of a Notice of Allowance of Claims 1-13 are requested.

If there are any fees due in connection with the filing of this response, please charge those fees to our Deposit Account No. 02-2666. If a telephone interview would expedite the prosecution of this Application, the Examiner is invited to contact the undersigned at (310) 207-3800.

Respectfully submitted,

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Dated: February 28, 2005

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Linda Marie D'Elia 2/28/05

Linda Marie D'Elia February 28 , 2005